

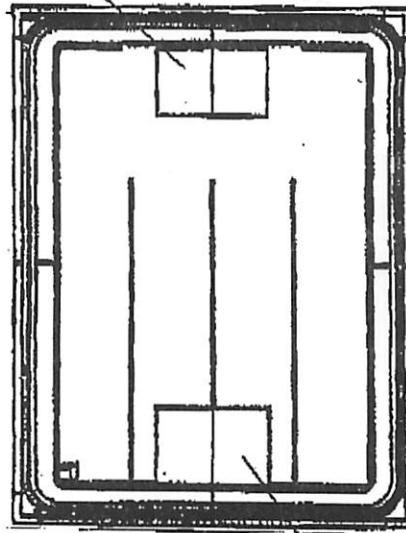


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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

SOURCE



GATE

CHIP BACK IS DRAIN

Topside Metal: Al
Backside: AlTiNi
Backside Potential: Drain
Mask Ref: Issue 1
Bond Pads : .004"

APPROVED BY: CB
MFG: Harris

DIE SIZE : .182" x .126"
THICKNESS: .014"

DATE: 2/7/01
P/N: IRFC130

DG 10.1.2
Rev A 3-4-99